

G31T-LS

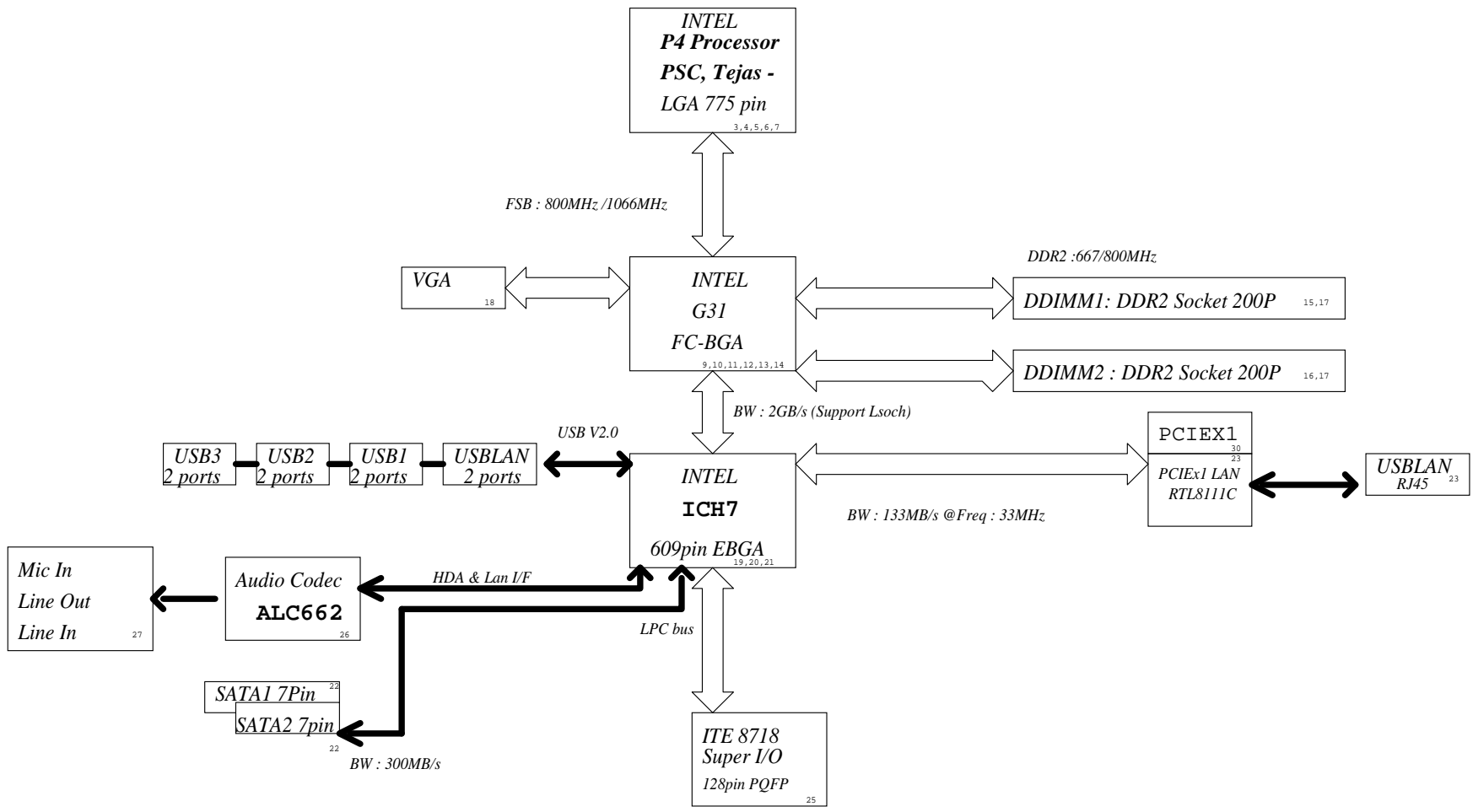
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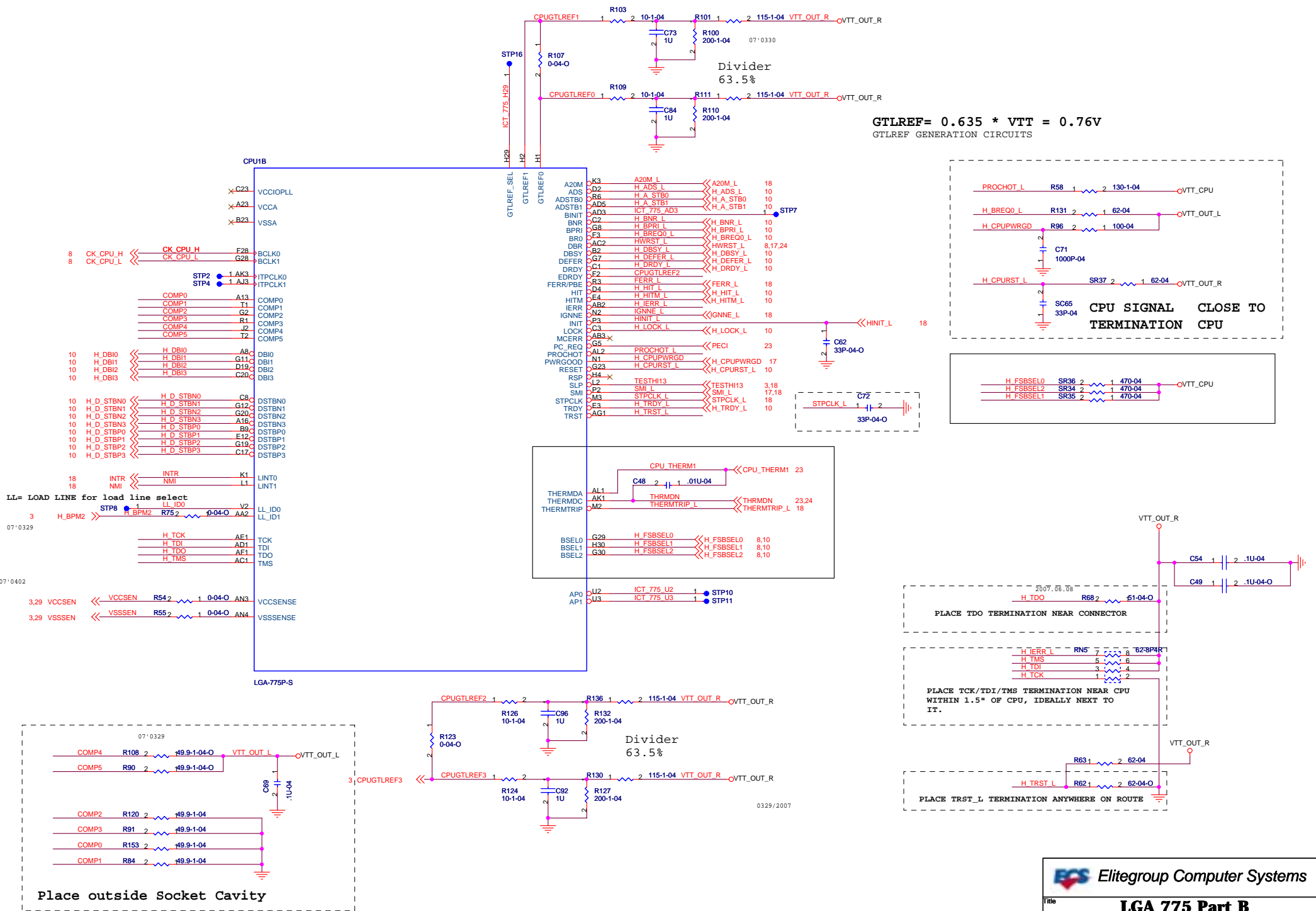
Reversion History

Rev: 0.1	2007/11/27	First Release
Rev: 0.2	2008/01/11	First Release
Rev: 0.3	2008/02/22	First Release
Rev: 1.0	2008/04/09	First Release

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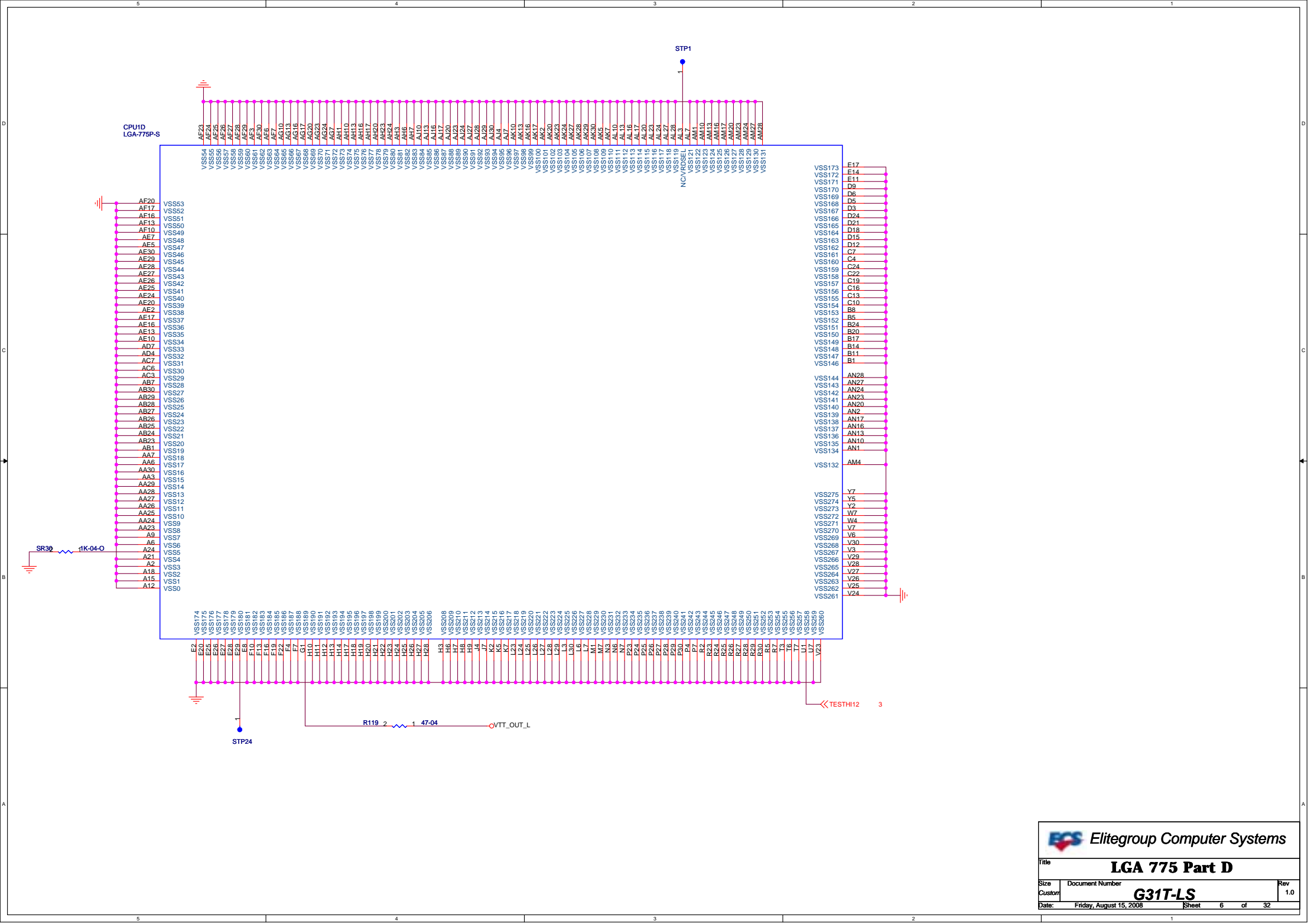
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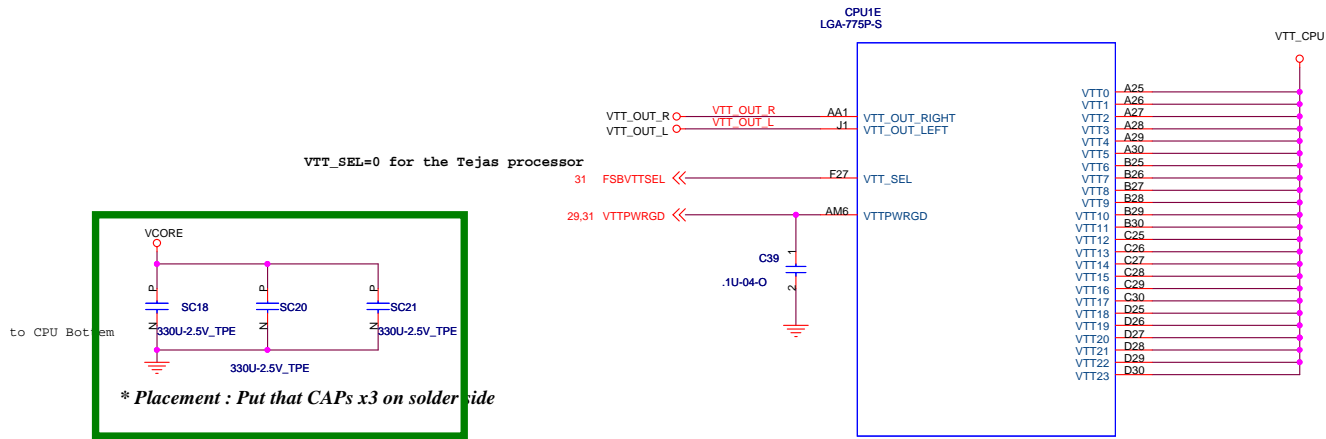
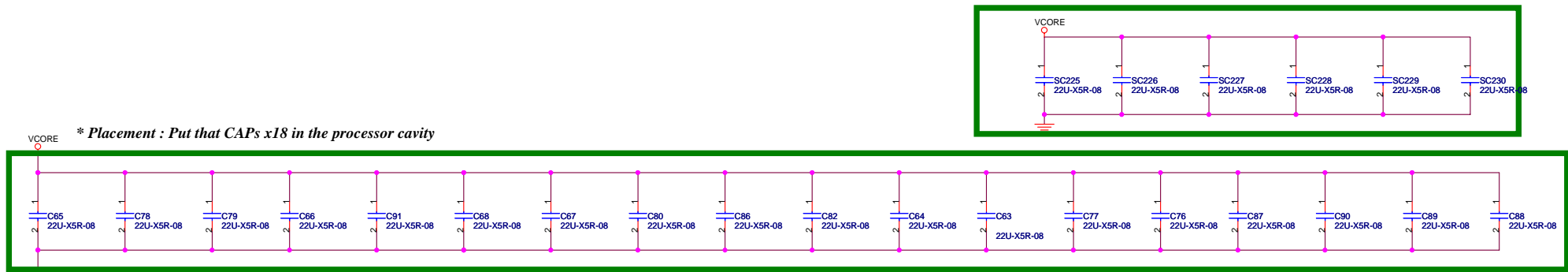


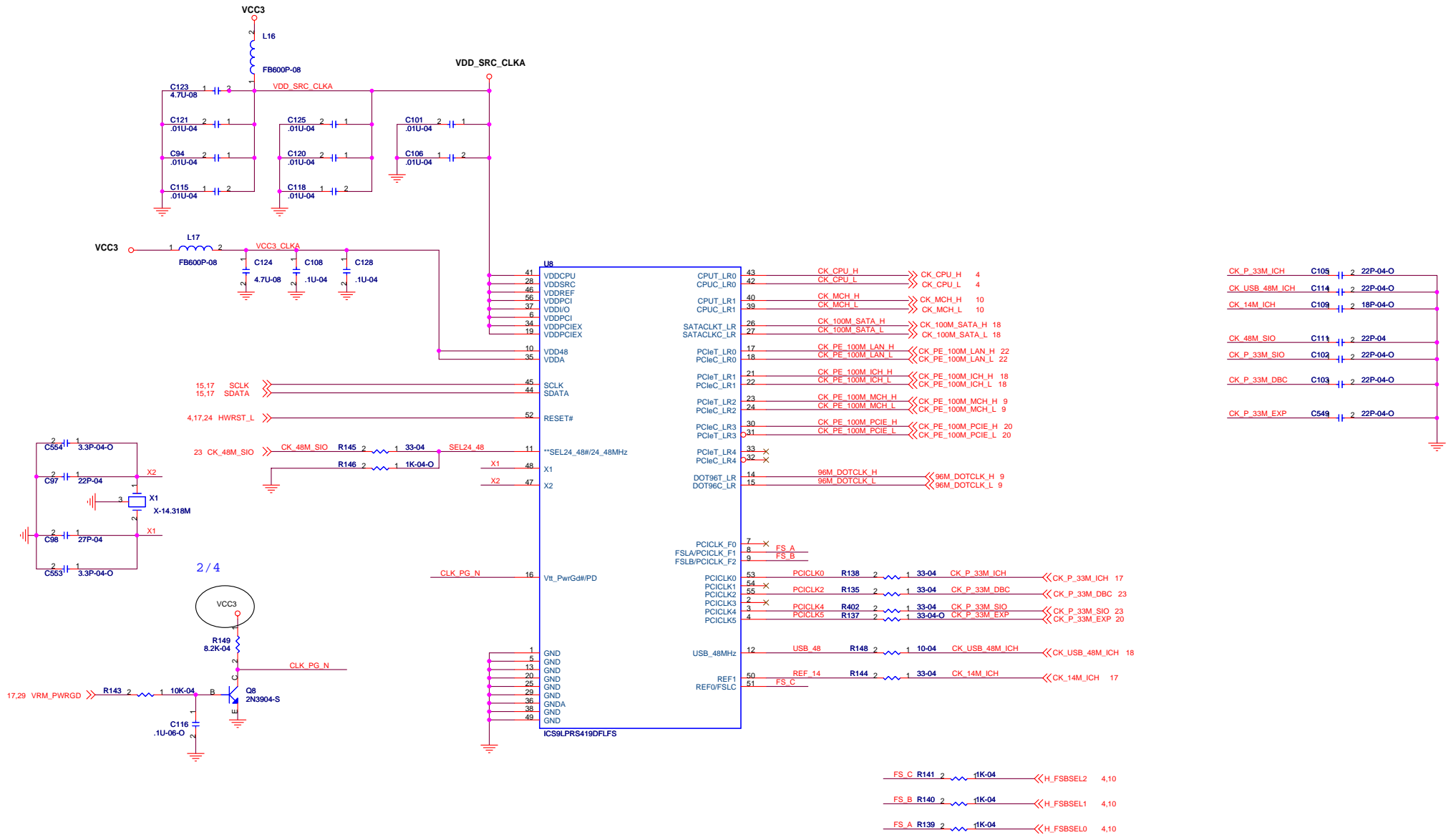




CPU1C
LGA-775P-S







FS C R141 2 1K-04 <<H_FSBSEL2 4,10

FS B R140 2 1K-04 <<H_FSBSEL1 4,10

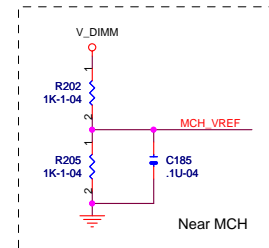
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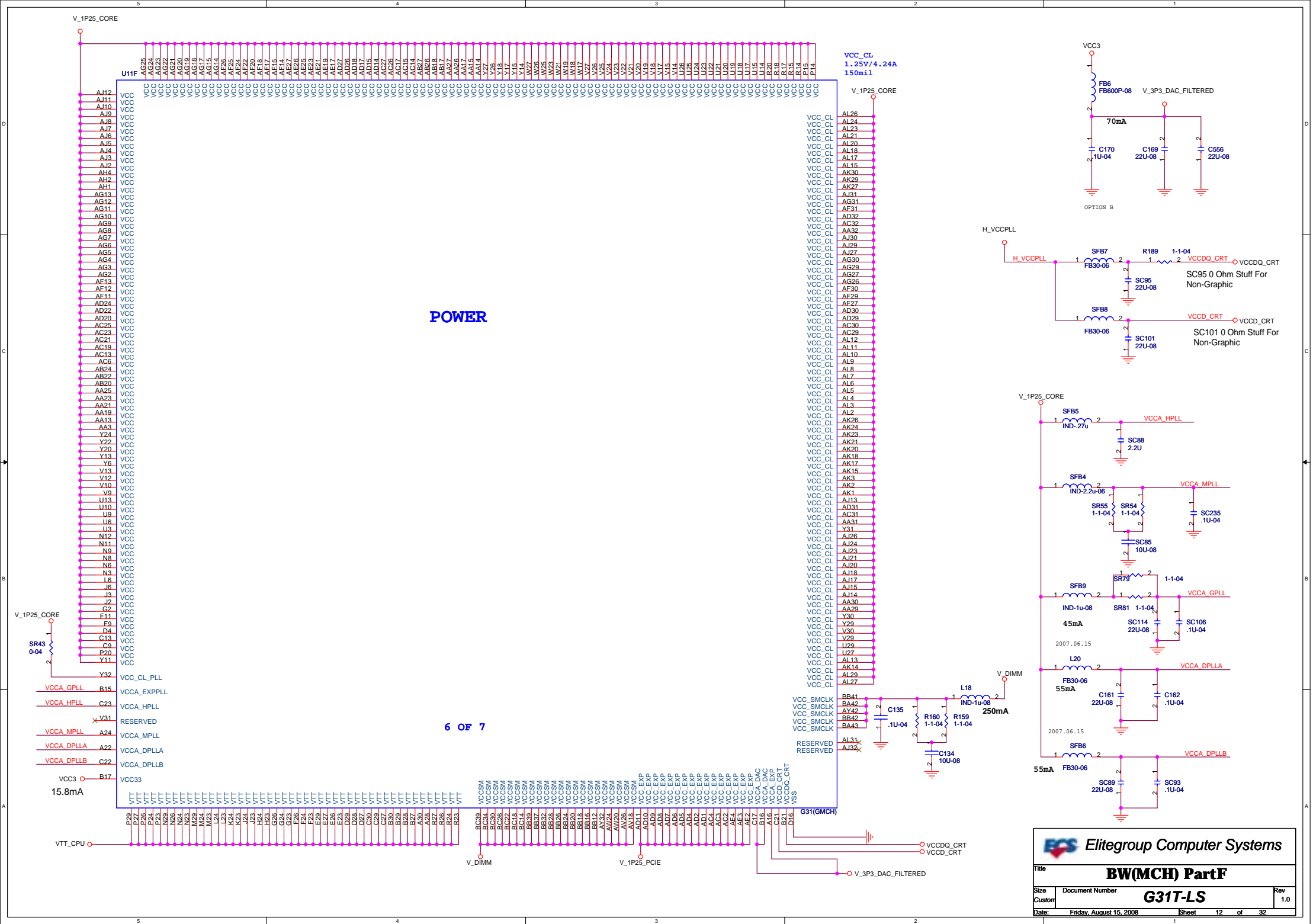
BSEL TABLE	
2 1 0	FSB FREQUENCY
0 1 0	200 MHZ (800)
0 0 0	266 MHZ (1066)

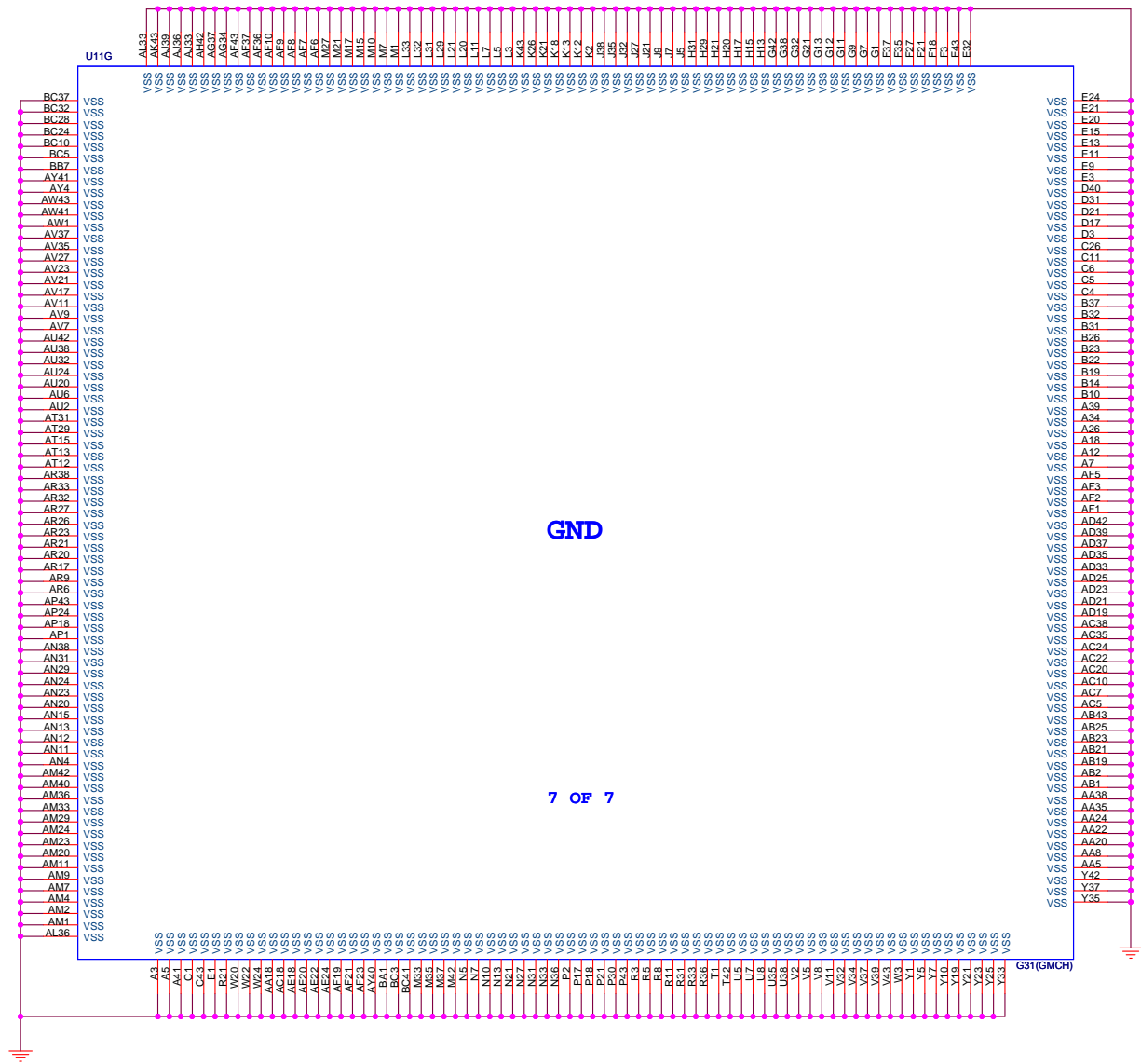
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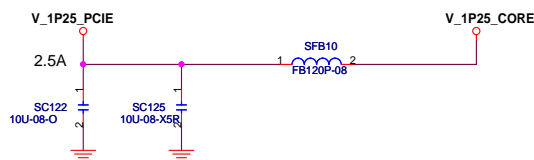
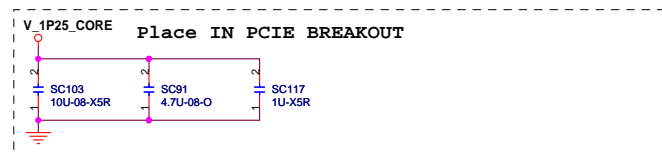
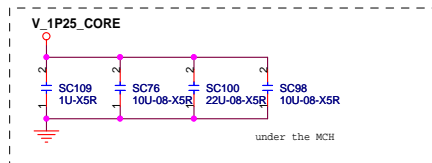
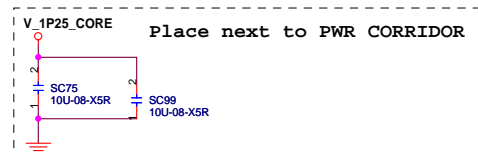
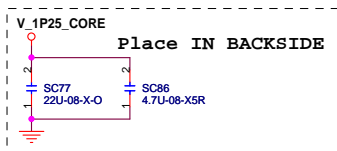
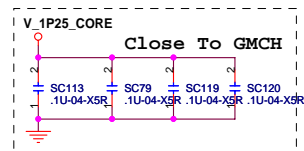
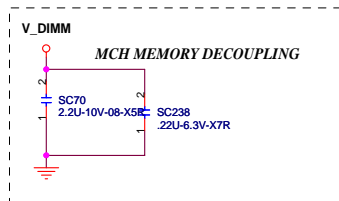
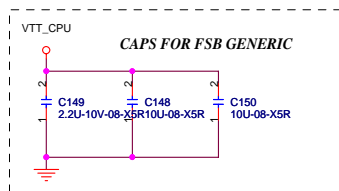
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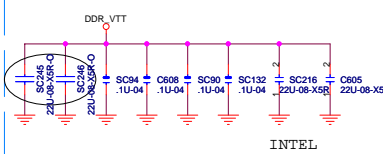
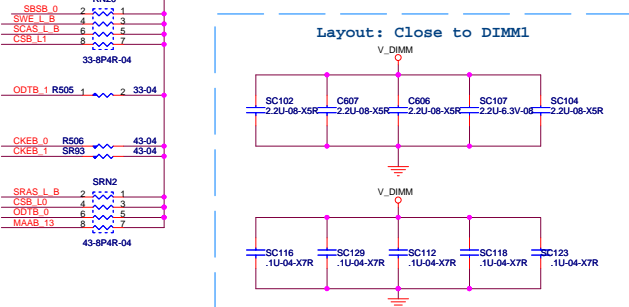
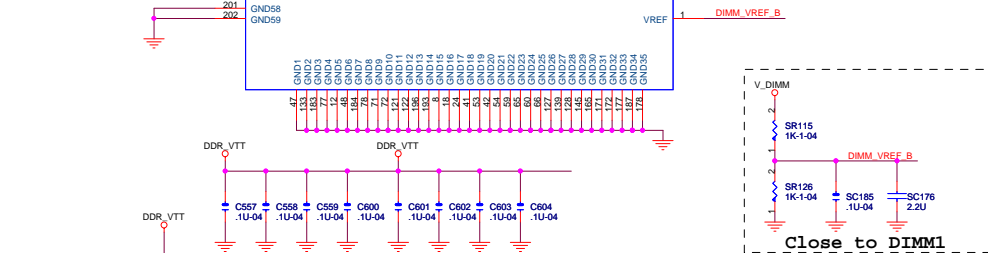
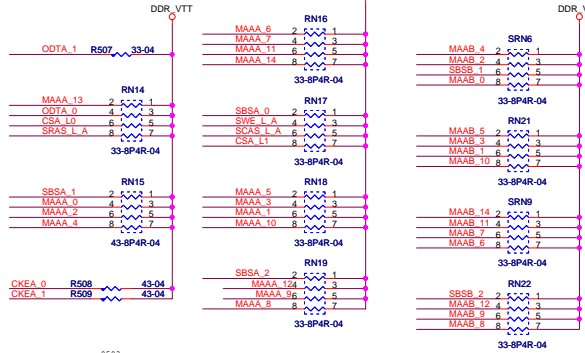
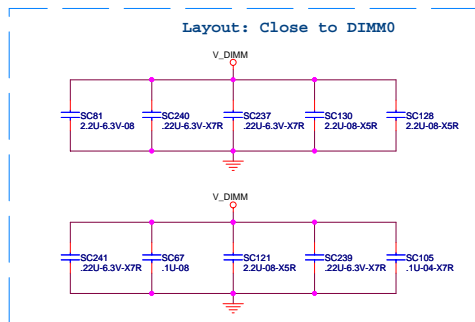
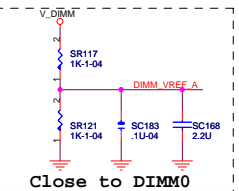
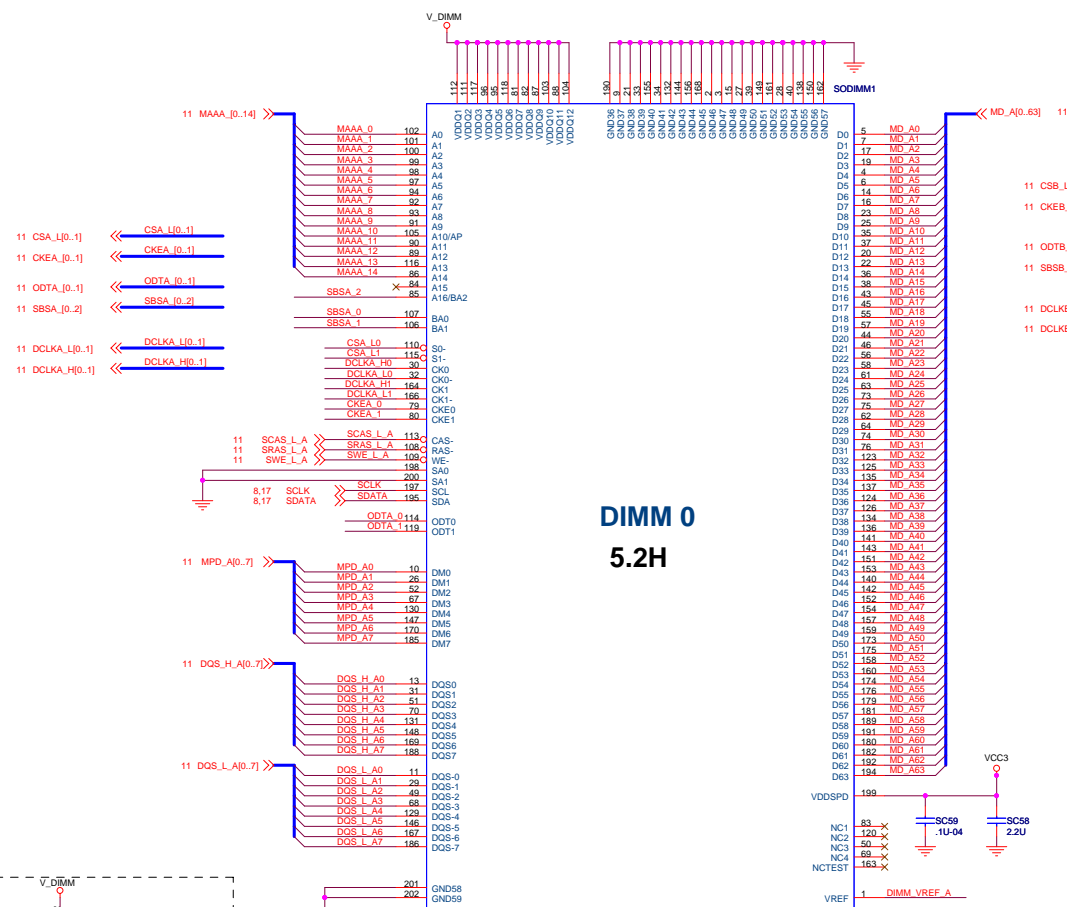




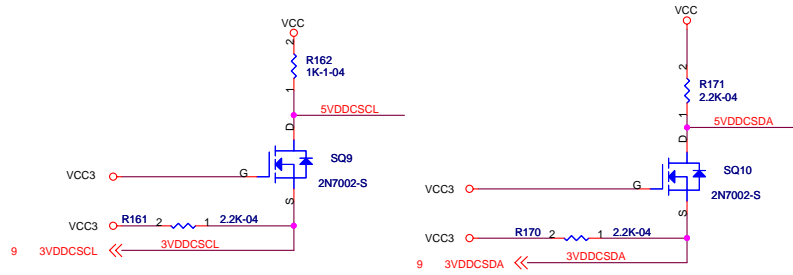
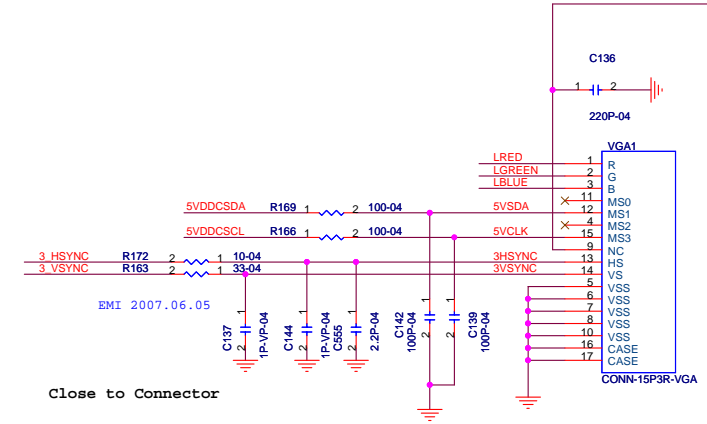
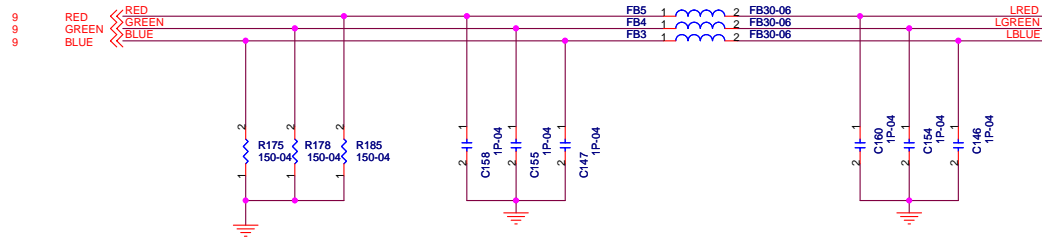


2116 : trace width 5 mil 60 ohm
Trace Length 3500 mils
Spacing: 1.clearance to itself 20/5/20(S:W:S)
2.clearance to other signal 3W

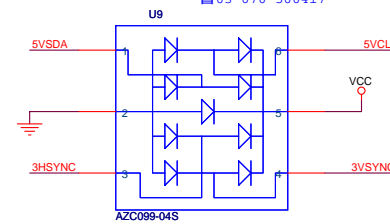
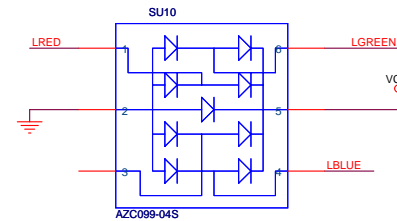
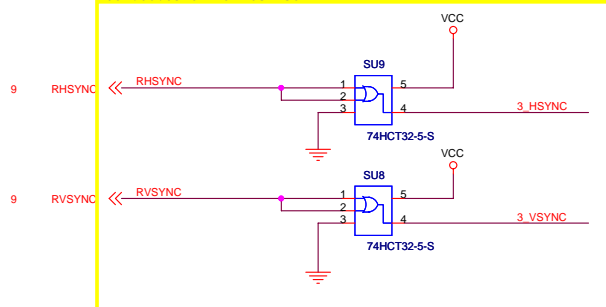
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Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W



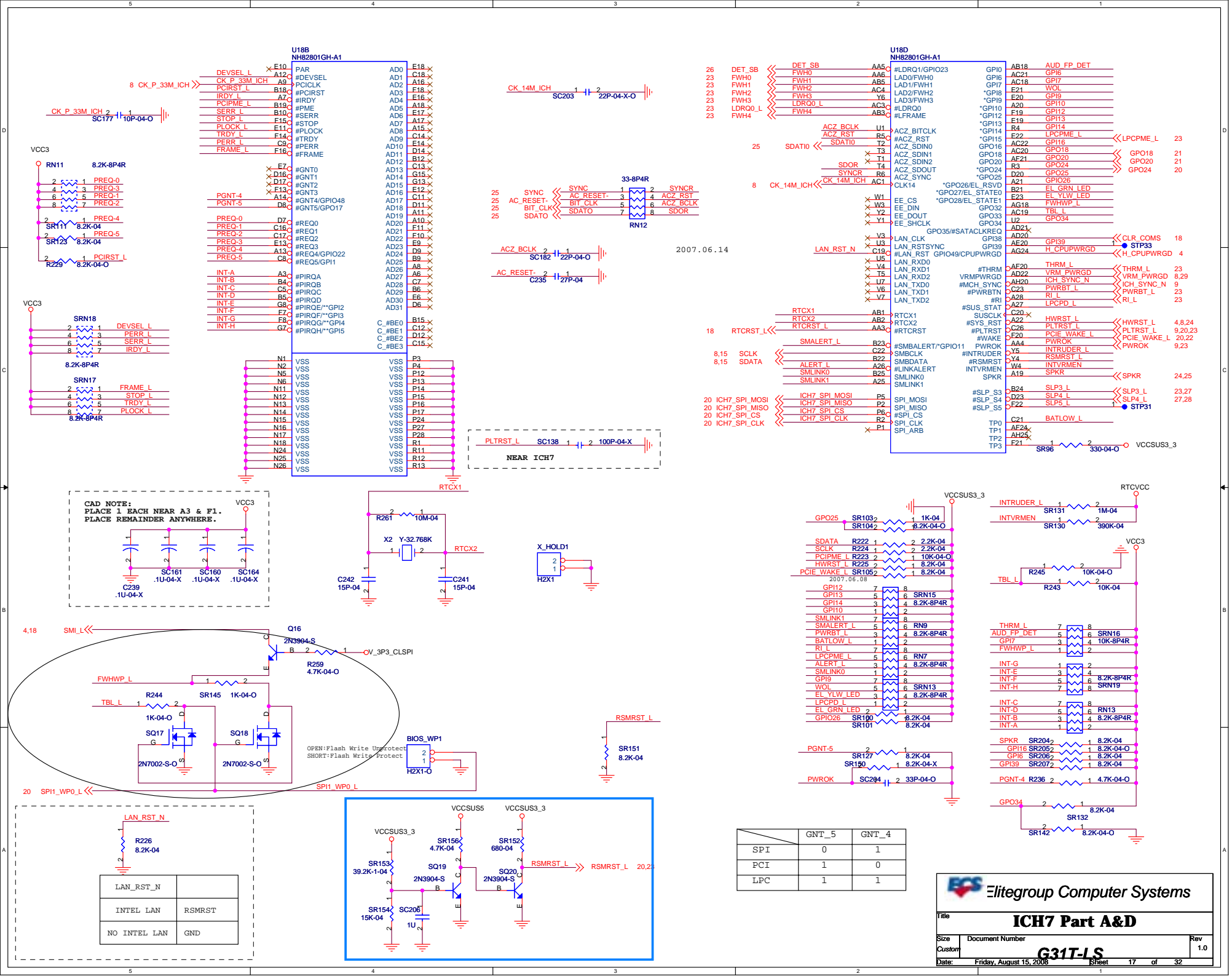
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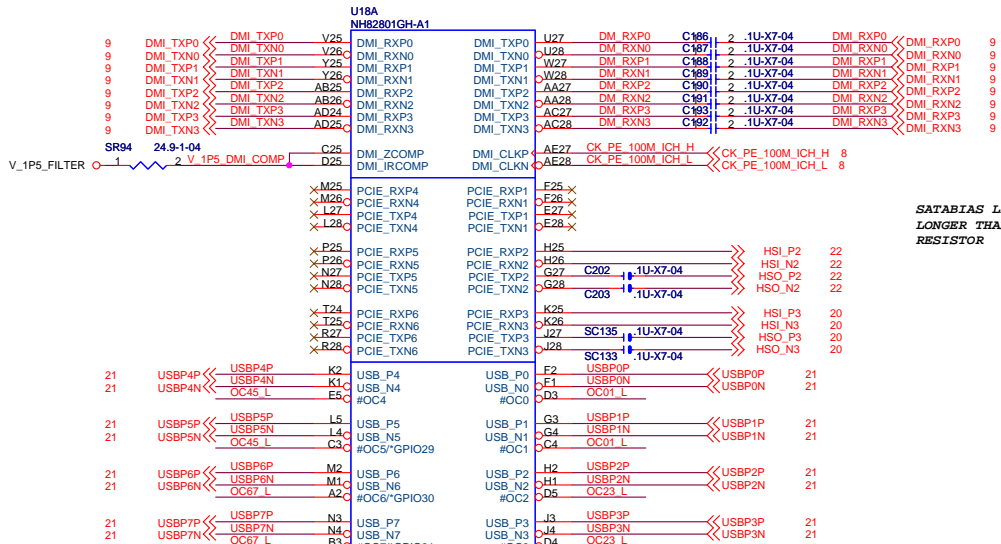


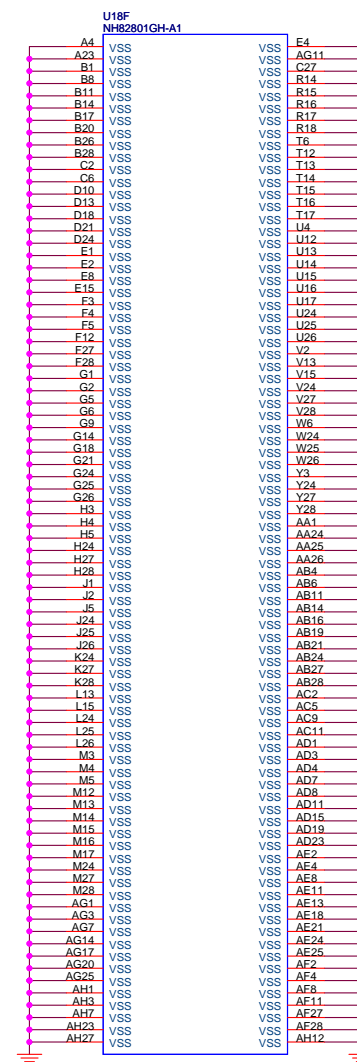
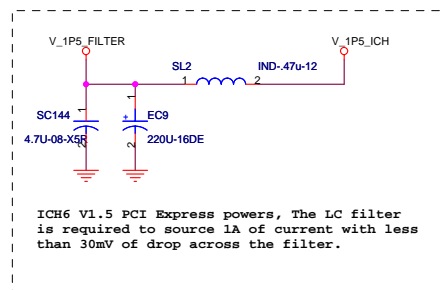
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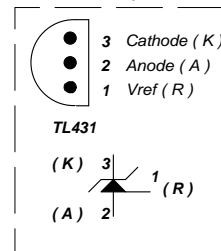
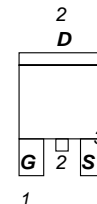
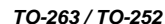
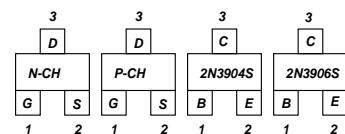
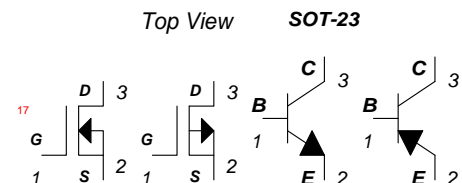
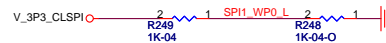
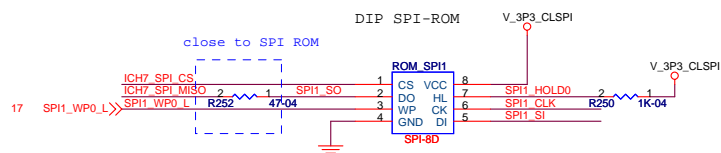
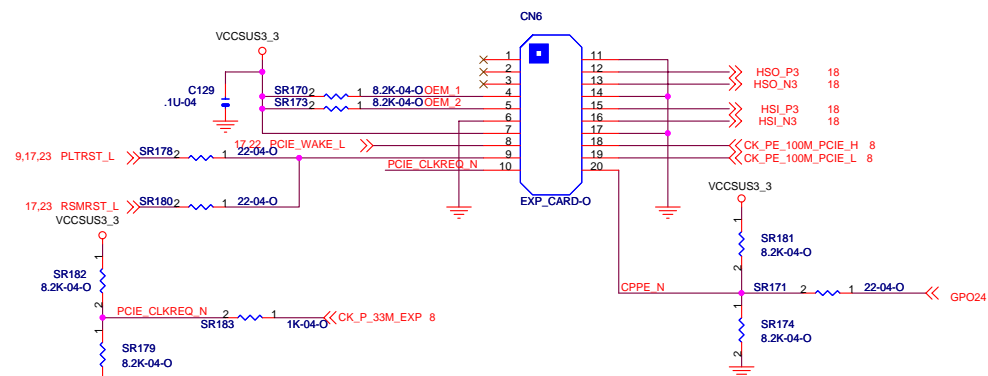
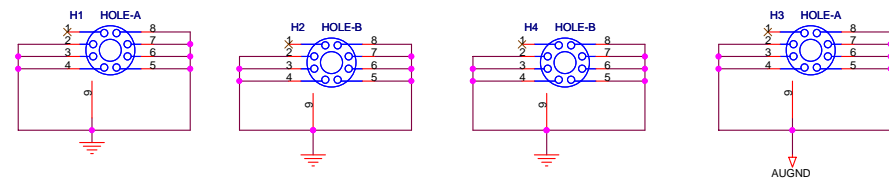


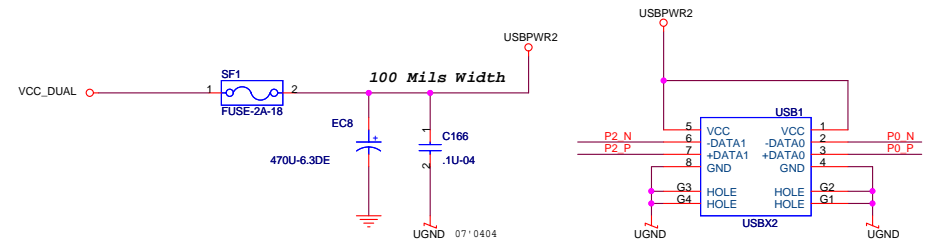
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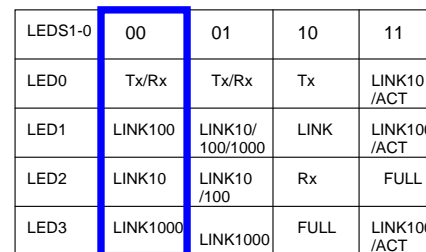
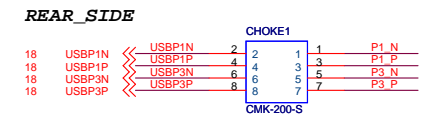
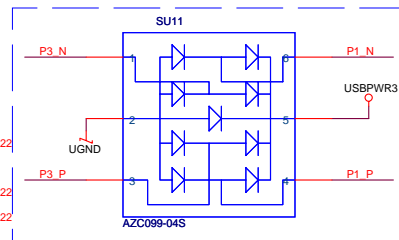
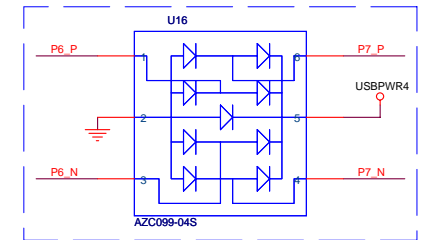
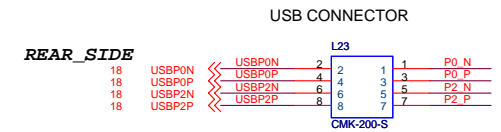
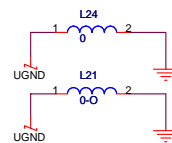
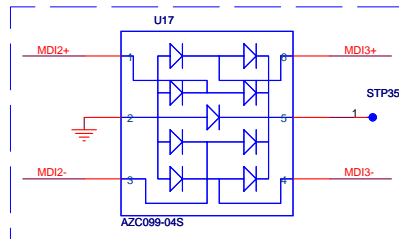
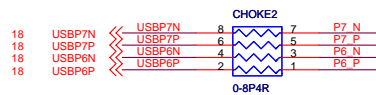


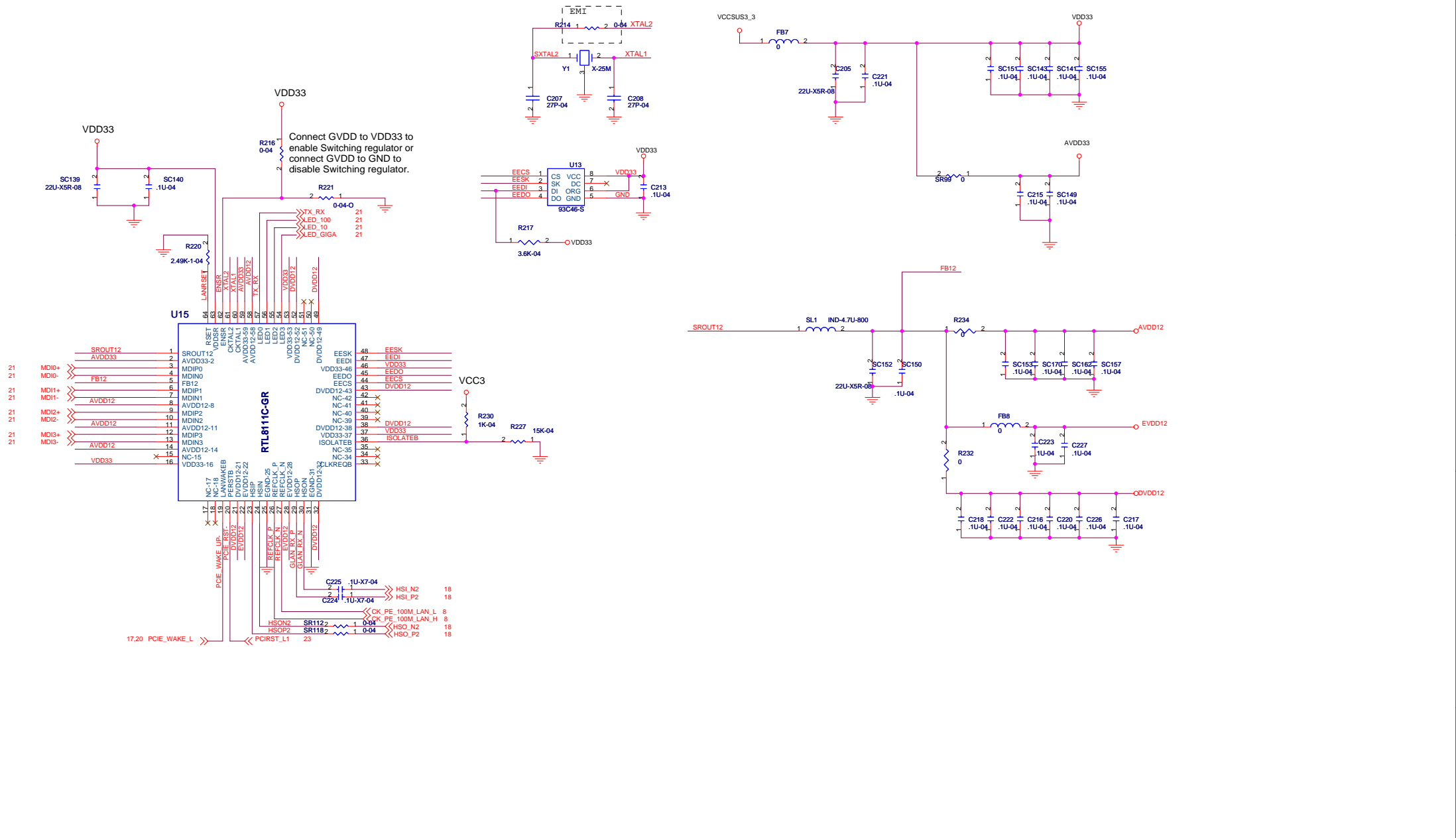


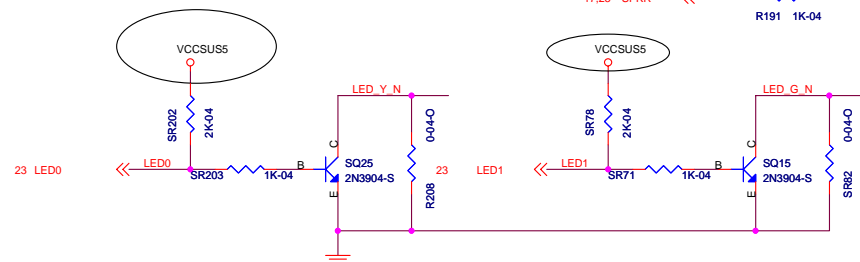
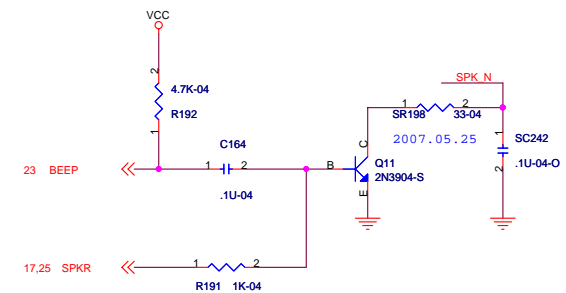
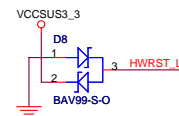
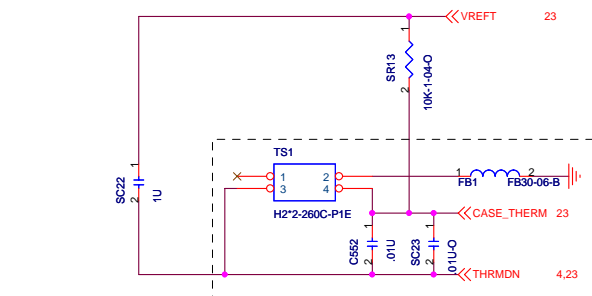
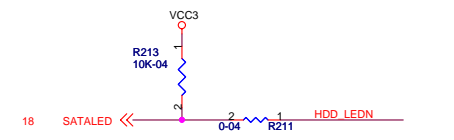
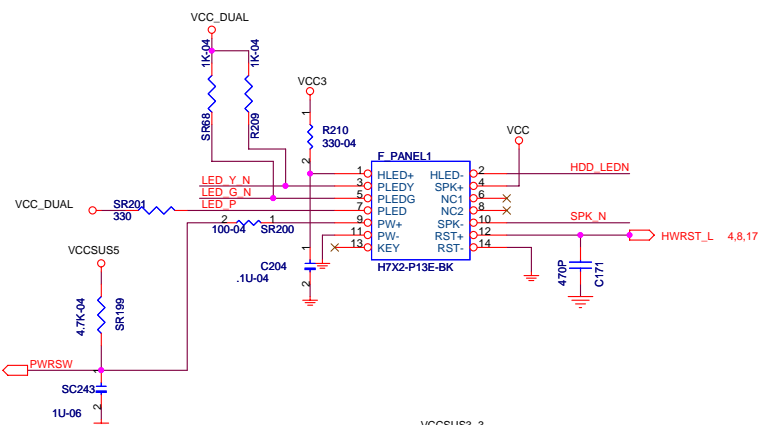
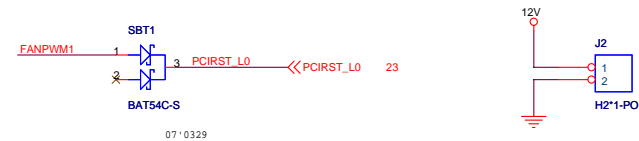


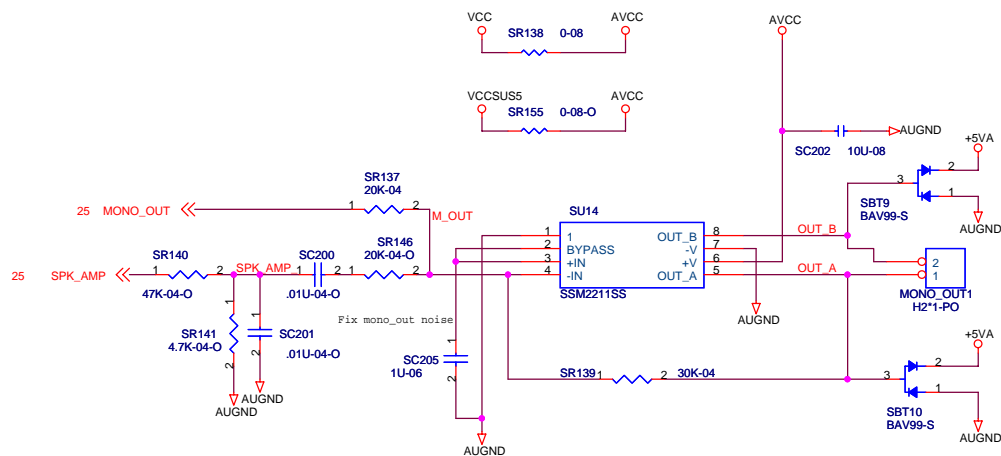
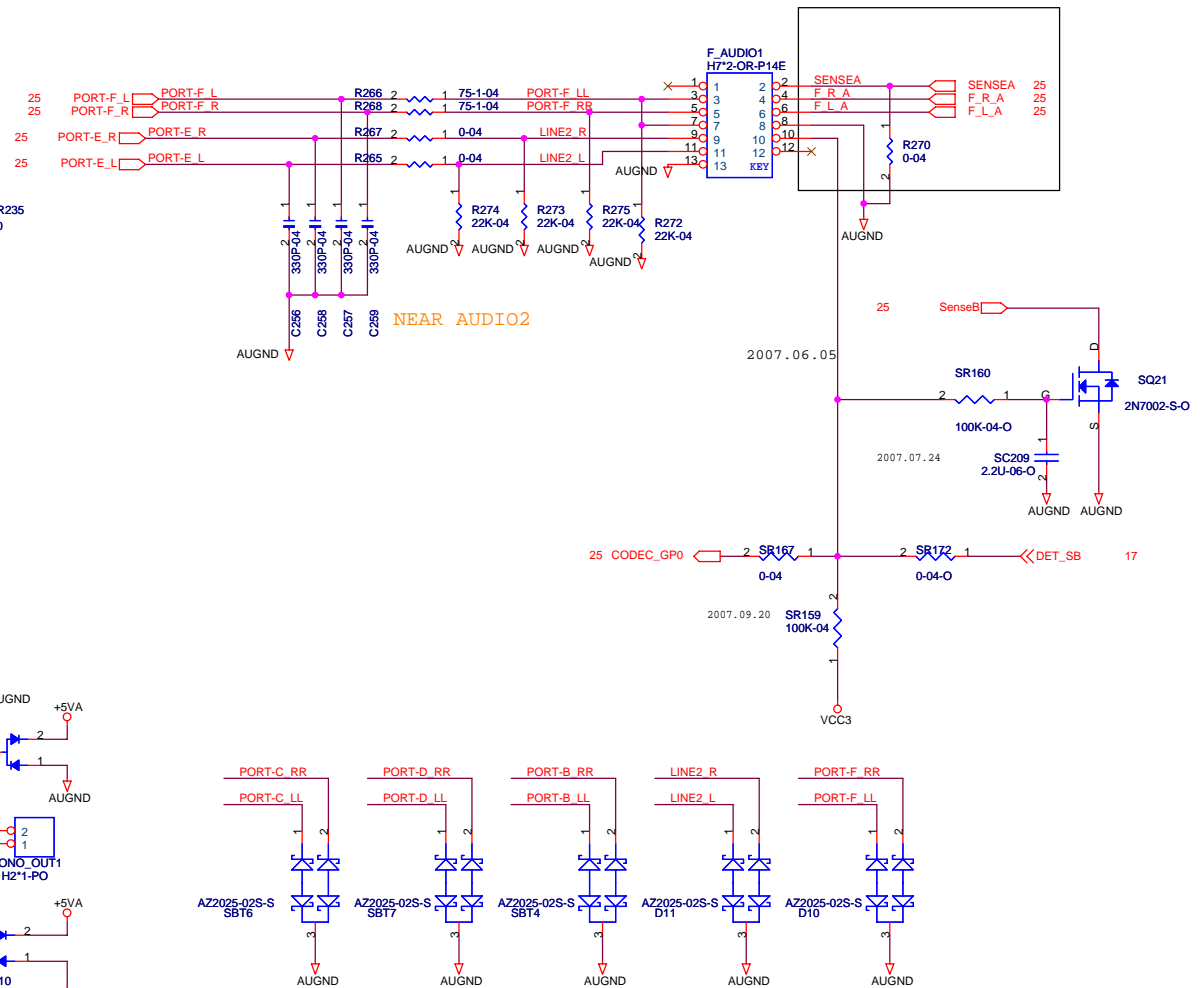
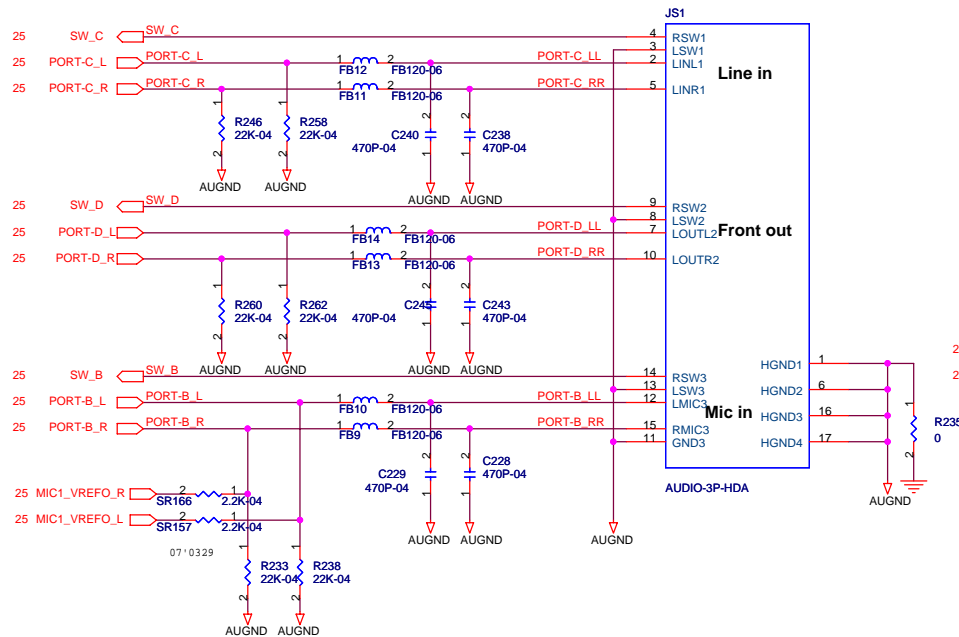


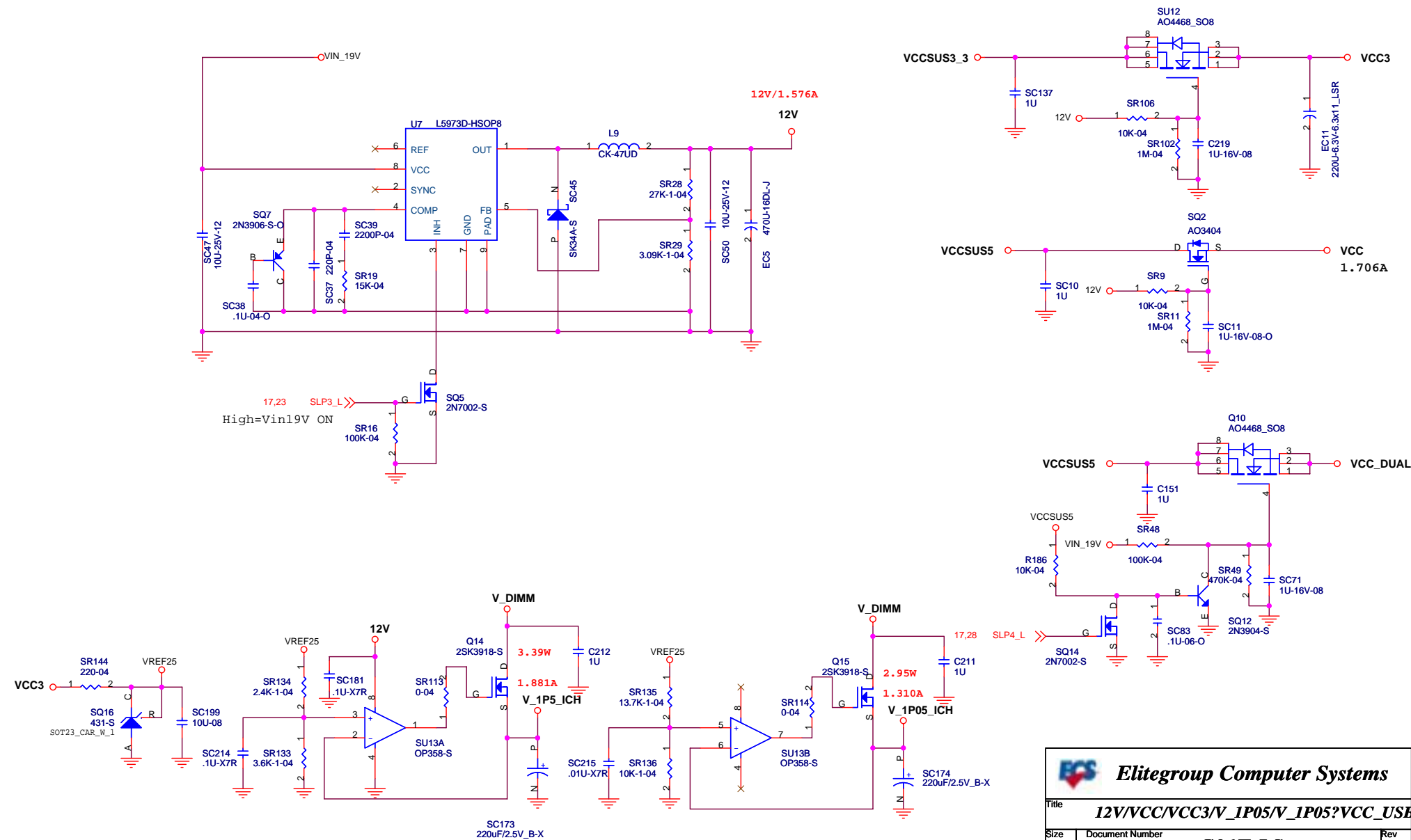
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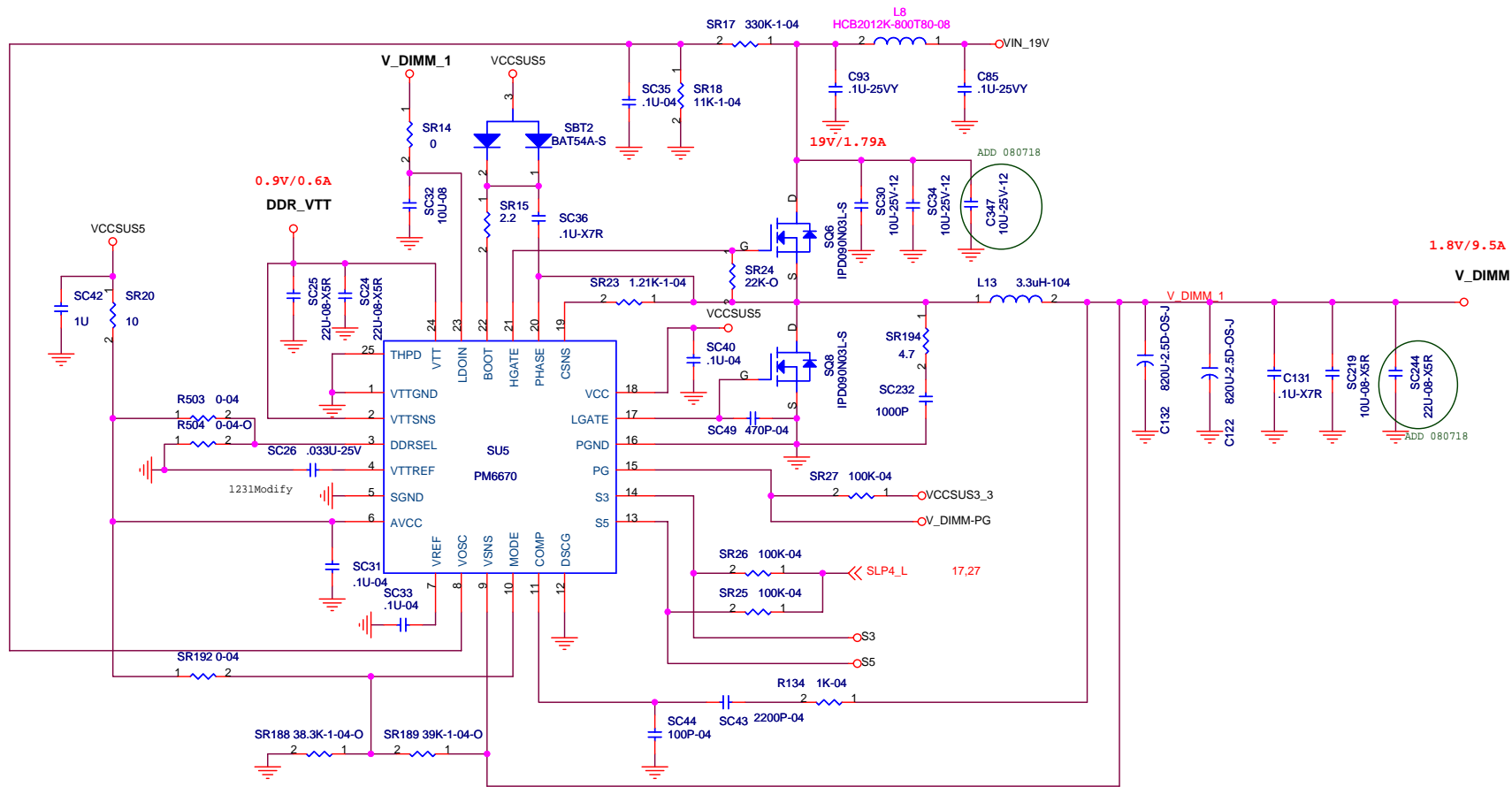




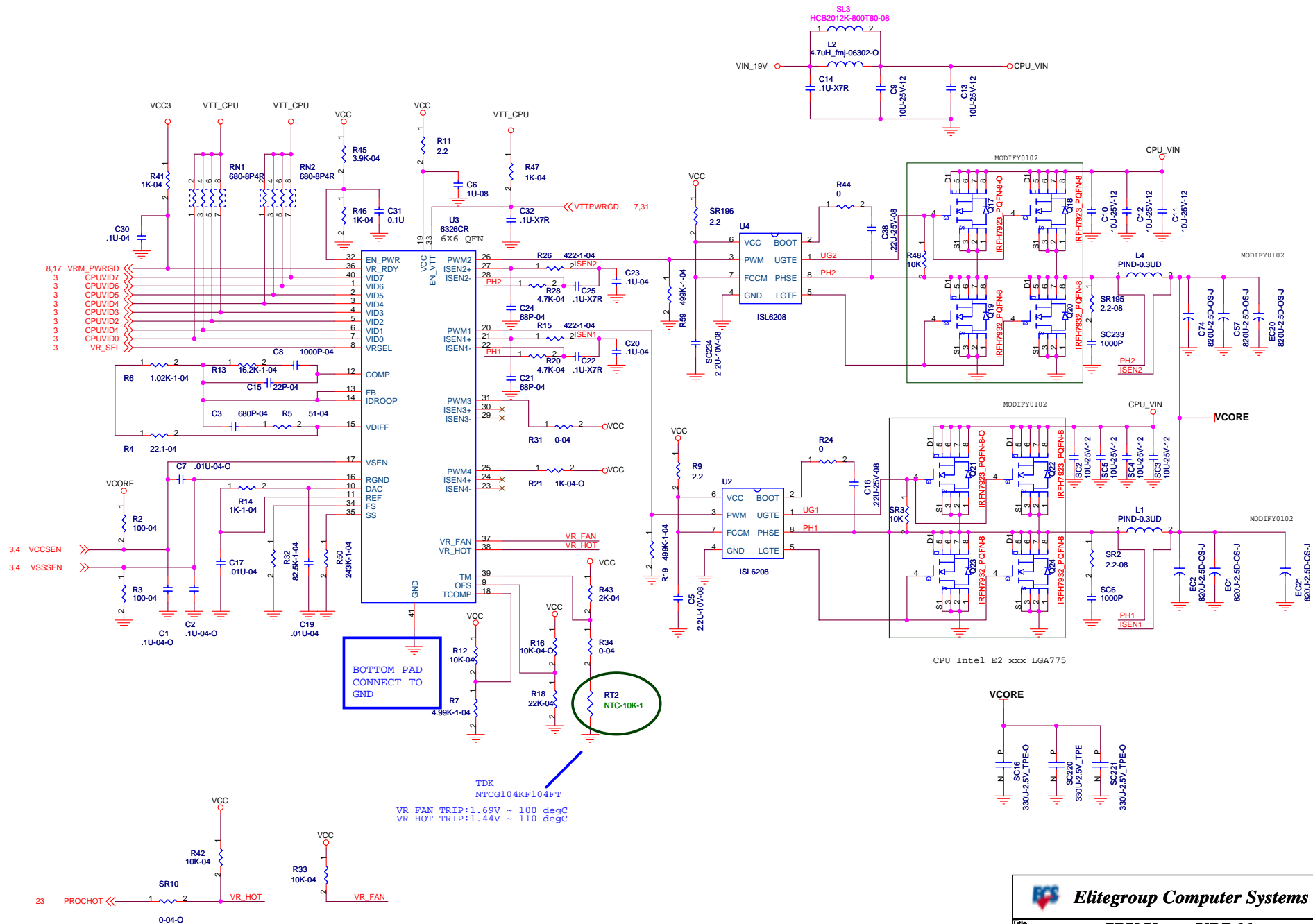


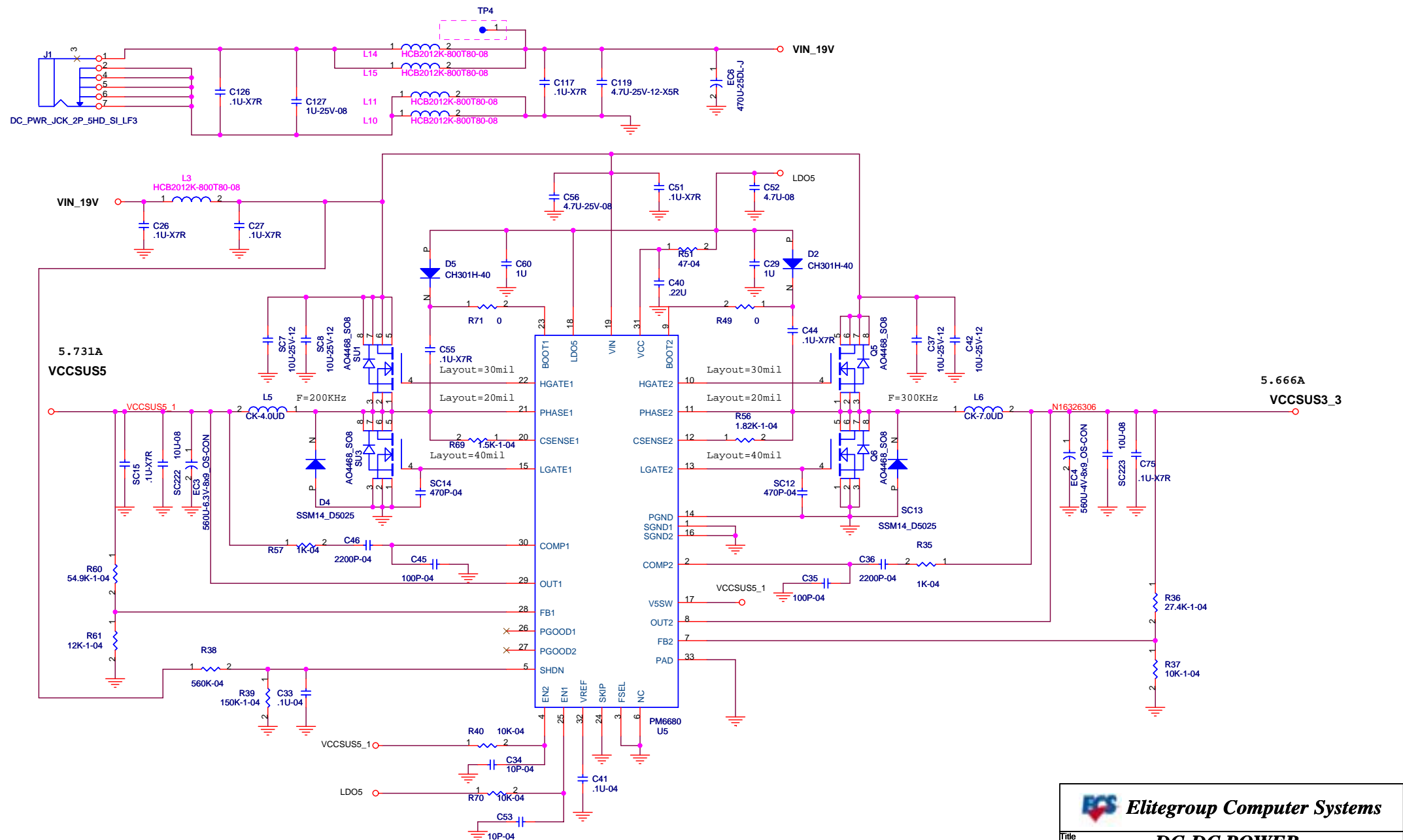






I SL6326CR FOR Intel P4 Conroe VRD11 POWER CKT





Ver 0.1

1 P.20 add CN6 (EXPRESS CARD) CKT
2 P.21 add SQ22, SQ23, SQ24 LAN LED CKT
3 P.23 add RT1, RT3 CKT
4 P.24 add J2 LED header CKT
5 P.24 change 3pin CPU FAN
6 P.26 add MONO_OUT header CKT
7 P.27 change ST 12V solution
8 P.28,30,31 add Z1,Z2,Z3,Z4,Z5 for power rail break point
9 P.29 change VCORE CKT for FMB06

Ver 0.2

1 P.12 change SFB6,SFB7,SFB8,L20, (FB120→0 OHM...SMD 0603) for VGA power quality.
2 P.16 change FB3,FB4,FB5 (FB.80→FB30 OHM.25%...SMD 0603) for VGA signal quality.
3 P.16 change R162 (2.2K→1K...SMD 0402) for VGA DDC signal quality.
4 P.20 change R36 (26.7K →27.4K 1%...SMD 0402) in order to rise VCCSUS3_3 voltage to 3.34V
5 P.22 modify FB7 PU VCCSUS3_3, ADD R217 to 3.6K 0402, R227 15K 0402 in order to enable WOL function.
6 P.23 reserve CN1 HW debug port, (10-261-012382 HEADER.BV..12*1 180D)
7 P.25 stuff R239 0 ohm 0402, R240 4.7K 0402, C230 0.01uF 0402, C233 0.1uF 0402 in order to enable PC BEEP function.
8 P.03 stuff SC65 (33pf...SMD 0402) fo CPURST_L signal quality.
9 P.18 change SR143 (22.6→22.1 OHM...SMD 0402) for USB EYE pattern.
9 P.18 stuff SC206 (1uF...SMD 0603) for RSMRST timing spec.
10.P.17 add C553, C554 (3.3pF...SMD 0402) for 14.318M timing.

Ver 0.3


1 P.29 DEL SQ3, Resrve SR10, in order to fix signal 5V level and reserve no function ITE GPIO.
2 P.30 DEL SFB2, SC46, SC48, change EC6 (330uF→470uF) in order to reduce 19V power noise.
3 P.30 modify VCC1.5V, VCC1.05V regulator power source (VCC3-V_DIMM; Q14, Q15 pin.D-V_DIMM, SR144.pin1VCCSUS3_3-VCC3) for Q14, Q15 thermal issue.)
4 P.29 modify & reserve L2-08-413-475370 4.7uH_choke to reduce VGA noise, add SL3 (HCB2012K-800T80)
5 P.20 modify ROM_SPI1(SMD-DIP) for RMA work suggestion
6 P.20 del trace SPI1_WP0_L, from ROM-SPI1.pin3 to U6.pin18 (IT8718F-S GX-LG P31)→SR196,
7 P.12 add SC235 0.1uF; add C555 2.2pF; change C169 (10uF→22uF); SC95, SC101 (0.1uF→1uF);L20, SFB6, SFB7 (0 OHM→FB.30); SFB8 (FB.120→FB.30); stuff SC89, SC114, C161 22uF;
8 P.23 modify R65.pin1 connect trace N_RIA in order to RS232 R/I issue.
9 P.17 add X_HOLD1 to reduce thermal effect of X'TAL 32.768K.
10 P.30 change C33 (10pF→0.1uF 0402) for rush current protect.
11 P.18 modify SATA1 to SATA2 (U18.AE7, U18.AF7, U18.AG6, U18.AH6) in order to fix SATA compatite mode fail
12 P.12 add SC235 0.1uF; add C555 2.2pF; change C169 (10uF→22uF); SC95, SC101 (0.1uF→1uF);L20, SFB6, SFB7 (0 OHM→FB.30); SFB8 (FB.120→FB.30);
13 P.03 stuff SC60 22uF to reduce VGA noise;
14 P.21 stuff SC169 470pF for EMI test;
15 P.24 add SR197 15K, SC236 22UF, stuff R406 4.7K fix smart Fan issue;
16 P.08 change R148 → 10 ohm, reserve C148 for 48M CLK signal quality
17 P.21 modify U14, U17 pin1 connect test point for WOL leakage issue.

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17 P.21 unstuff C553, C554; change C98 → 27pF

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1 P.24 modify R199 &SR78 pin1 connect VCC_DUAL to VCCSUS5 for VCC_DUAL electric leakage
2 P.23 modify R98 pin1 connect VCCSUS5 to VCC for VCC electric leakage
3 P.23 modify SU4.26 and SR12.1 connect VCCSUS5 to VCC for VCC electric leakage
4 P.15 add&reserve SC245,SC246 (22uf) for DDR_VTT Power Quality
5 P.28 add C347(10uf) and SC244(22uf) for V_DIMM Power Quality
6 P.17 unstuff R259,SR145,R244,SQ17,SQ18,BIOS_WP1 for not use Flash write Protect function

 Elitegroup Computer Systems			
Revision History			
Title			
Size	Document Number	Rev	
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